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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,855	03/30/2004	Hannu Ventomaki	915-007.083	5601

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EXAMINER	
NGUYEN, JIMMY	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 06/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/814,855	VENTOMAKI, HANNU	
	Examiner	Art Unit	
	Jimmy Nguyen	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5, 7 - 34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5, 7 - 34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Argument

The RCE filed 5/11/06 has been carefully considered with the following effect;

First, the applicant's amended limitation added the mobile phone comprising in the pre-amble of the claim, however, the pre-amble of the claim is the intended use only and it will not be considered during the examination.

Further, the applicant argues that there is no connector is used for connecting the IC package to the circuit board but rather, the present invention discloses the use of support elements directly connecting IC package mechanically with circuit board using solder board (page 8 of the remark). The examiner is respectfully traversed this argument. As indicated by the applicants, the support elements directly connecting IC package mechanically with the circuit board, therefore the support elements are another form of the connector (either physically or electrically) between the IC and printed circuit board.

In view of the foregoing, it is respectfully submitted that the present applicant as amended is not overcome the prior arts of rejection.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 – 5, 7 - 34 are rejected under 35 U.S.C. 102(e) as being anticipated by Barr et al (US 2004/0257090)

As to claims 1, 30, 34, Barr et al disclose (figs 1, 2, 6) a method for analyzing connection conditions between an integrated circuit package (daughter board , column 1 paragraph 20) and a circuit board (mother board, column 1 paragraph 20) comprising step of

electrically coupling said integrated circuit package (daughter board , column 1 paragraph 20) to said circuit board (mother board, column 1 paragraph 20) by coupling elements (102),

mechanically connecting IC (daughter board) with said circuit board (mother board) by support elements (pins 1 and 2 of daughter board, fig 2)

electrically connecting (fig 2) at least two of support elements (pins 1, 2) with each other on the side of IC package

picking off physical values (fig 6, by 104) to determine mechanical properties if support

concluding (by 104) a condition of electrical coupling of IC package with circuit board from determined mechanical properties of support element.

As to claim 2, Barr et al disclose (figs 1, 2, 6) the electrical values (by 104 column 2 paragraph 24) are pick off from support elements (pins 1, 2).

As to claim 3, Barr et al disclose (figs 1, 2, 6) the electrical current (by 104 column 2 paragraph 24) within the support element (pins 1, 2) is picked off.

As to claims 4, **5**, Barr et al disclose (figs 1, 2, 6) the mechanical values (the joint solder are making sure the pins are connected) are picked off from support elements (pins 1, 2) by using the strain gauge (transmission lines).

As to claim 7, Barr et al disclose (figs 1, 2, 6) the connection condition is determined in intervals (paragraph 22).

As to claims 8 – 12, **22**, **24 – 26**, Barr et al disclose (figs 1, 2, 6) determined connection condition is determined , store and presented on a user interface (106) , a error message is generated (to the system management).

As to claims 13, **27**, Barr et al disclose (figs 1, 2, 6) a system for analyzing connection conditions between an integrated circuit package (daughter board) and a circuit board (motherboard) comprising:

coupling elements (102) coupling said integrated circuit package (daughter board) electrically to said circuit board (motherboard), and

support elements (pins 1, 2) connecting said integrated circuit package (daughter board) mechanically with said circuit board (motherboard), wherein the system further comprising:

means electrically connecting at least two support elements (pins 1, 2) with each other on the side of the IC package (fig 2)

measuring (by 104) means arranged at said support elements (pins 1, 2) for picking -off physical values between said support elements, and

evaluation (by 104) means for evaluating said physical values to determine mechanical properties of support elements (pins 1, 2), and for concluding a condition of electrical coupling of IC package with circuit board (determining the continuity) from determined mechanical properties of support elements

As to claim 14, Barr et al disclose (figs 1, 2, 6) the support elements (pins 1, 2) are arranged between circuit board (mother board) and IC package (daughter board).

As to claim 15, Barr et al disclose (figs 1, 2, 6) the support elements (pins 1, 2) are solder pads elements (or pins)

As to claim 16, Barr et al disclose (figs 1, 2, 6) the support elements (pins 1, 2) are arranged adjacent to coupling elements (102).

As to claims 17, **31**, **34,** Barr et al disclose (figs 1, 2, 6) the support elements (pins 1, 2) are arranged semicircular along coupling elements (102).

As to claims 18, **32**, Barr et al disclose (figs 1, 2, 6) the support elements (pins 1, 2) are arranged along edges and or at corners of IC package (daughter board).

As to claim 19, Barr et al disclose (figs 1, 2, 6) IC package (daughter board) is a CSP of chip (paragraph 20).

As to claims 20, **21**, Barr et al disclose (figs 1, 2, 6) the means of measuring electrical and mechanical condition of support element (pins 1, 2).

As to claim 23, Barr et al disclose (figs 1, 2, 6) the evaluation means compare picked off physical values with comparative values to determine the connection condition (voltage level, paragraph 22)

As to claims 28, 29, Barr et al disclose (figs 1, 2, 6) the computer program and product system (302) to cause a processor to analyze connection conditions between the IC package and a circuit board.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jimmy Nguyen whose telephone number is 571 – 272-1965. The examiner can normally be reached on Monday - Friday from 9am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen, can be reached on 571-272-1678. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jimmy Nguyen

JN.
May 26, 2006

VINH NGUYEN
PRIMARY EXAMINER
A.U. 2829
05/30/06